IN THE CLAIMS:

1. (Currently Amended) A computer processor having control and data processing capabilities comprising:

a decode unit for decoding instructions;

a dedicated control processing facility comprising a control execution path having its own control register file, a branch unit, an execution unit, and a load/store unit; and

a dedicated data processing facility, separate from said dedicated control processing facility, having its own data register file separate from said control register file, the data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators and a controller, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired operator classes;

wherein said decode unit which separates control instructions from data processing instructions and is operable to detect whether one of said [[a]]data processing instruction defines a fixed data processing instruction or a configurable data processing instruction, said decode unit causing the computer processor to supply said data processing instruction to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when a configurable data processing instruction is detected; and

wherein said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction.

2. (Original) A computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of instruction packets from memory, each packet comprising a plurality of instructions.

3. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction.

4. (Original) A computer processor according to claim 1, wherein the configurable operators are configurable at the level of multibit values.

5. (Original) A computer processor according to claim 4, wherein the configurable operators are configurable at the level of multibit values comprising four or more bits.

6. (Original) A computer system according to claim 4, wherein the configurable operators are configurable at the level of words.

7. (Original) A computer processor according to claim 1, wherein a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles.

8. (Original) A computer processor according to claim 1, wherein a plurality of configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles.

9. (Original) A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the

nature of the operations performed.

10. (Original) A computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed from a field of an instruction defining a configurable data processing operation.

11. (Previously Presented) A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information comprising information controlling connectivity of the configurable operators.

12. (Previously Presented) A computer processor according to claim 9, comprising a control map associated with configurable operators of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto.

13. (Original) A computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators.

14. (Original) A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive either configuration information determining the nature of an operation to be performed or configuration information controlling interconnectivity from a source other than a configurable data processing instruction.

15. (Original) A computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is capable of executing data processing instructions with an execution depth greater than two computations before returning results to a results store.

16. (Original) A computer processor according to claim 1, comprising a switch mechanism for receiving data processing operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators.

17. (Original) A computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop.

18. (Original) A computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for supply to configurable operators of the second data execution path.

19. (Original) A computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate for supply to configurable operators of the second data execution path.

20. (Original) A computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and cross-lane permuters.

21. (Original) A computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions.

22. (Currently Amended) A method of operating a computer processor having control and data processing capabilities, said computer processor comprising a decode unit for decoding instructions; a dedicated control processing facility comprising a control execution path having its own control register file, a branch unit, an execution unit, and a load/store unit; and a dedicated data processing facility, separate from said dedicated control processing facility, having its own data register file separate from said control register file, the data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators and a controller, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired operator classes, the method comprising:

separating, with said decode unit, control instructions from data processing instructions;

decoding a plurality of instructions to detect whether at least one of said data processing instructions ~~instruction,~~ of said plurality of instructions, defines a fixed data processing instruction or a configurable data processing instruction;

causing the computer processor to supply said at least one data processing instruction to said first data execution path for processing when a fixed data processing instruction is detected

and to said second data execution path for processing when a configurable data processing instruction is detected;

configuring the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction; and

outputting results produced by said first data execution path when a fixed data processing instruction is detected and outputting results produced by said second data execution path when a configurable processing instruction is detected.

23.-29. (Cancelled)